...We *are* boundary-scan.

JTAG
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When does boundary-scan make sense

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When does Boundary-Scan Make Sense

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Introduction

In today's competitive and rapidly changing electronics market, the speed and effectiveness of product testing have a significant impact on your bottom line and time-to-market. This booklet contains the background information on boundary-scan, one of the most effective methodologies available today for testing and in-system programming. Managers and designers will find the facts needed to help them reach an informed decision on whether to include boundary-scan in their test and/or device programming strategy.

The choice of such a strategy is crucial to overall product success, involving many departments within the enterprise in the planning and execution. Moreover, these departments can benefit directly from the right choice: designers, prototype providers, factory personnel, test engineers, and the repair department all have a stake in and benefit from the test strategy and programming method that are adopted.

If any of the following situations apply to you, now may be the right time to consider using boundary-scan:

- Existing test methods, such as functional testing and in-circuit testing (ICT) which have worked well in the past, are losing their effectiveness, due to the impact of new technologies such as ball-grid arrays (BGAs) on electrical access to your circuit boards

- You need to make Design-For-Testability (DFT) an essential part of your design process, along with the need for a reliable method of knowing the test coverage and how to improve it

- You need to reduce the overall cost of testing without compromising product quality

- You have an unacceptable number of boards in your "bone-pile"— boards that fail functional test but can't be diagnosed and thus remain unrepaired

- You're still using off-line device programming methods but want to save costs, increase quality, and create more flexibility in the factory and in the field

- You're under pressure to shorten the time-to-market for new products

Many of the IC devices in use on your products may already support boundary-scan (or JTAG as some IC vendors call it), whether you're using it or not. For example, the PowerPCs of IBM and Motorola, programmable logic devices from Altera, Xilinx, Lattice and STMicroelectronics, digital signal processors (DSPs) from Texas Instruments, wireless processors from Qualcomm, most application specific ICs (ASICs), and many others fully comply with IEEE 1149.1. So, it's quite possible that you can easily tap into the power of boundary-scan to improve board testability, dismantle the bone-pile, speed up board design and prototype debug, and even perform in-system programming of flash memory and programmable logic devices via the boundary-scan chain.

Regardless of which part of the product life cycle you're involved in, this booklet can help you learn the hows of boundary-scan: how it works, how you can benefit, and how to get started.

Functional testing is the original method of testing electronics. In the early days of the electronic industry, many systems were simply assembled and the power was switched on. By checking the functionality of the system, the "test" was performed.

Today, some companies still have to work in this way. However, the growing complexity of modern systems has made functional test preparation a lengthy job, while the fault coverage of such test programs may remain unknown. Moreover, diagnosing faults found in functional testing can be very difficult, often requiring highly skilled technicians in manufacturing. For this reason, testing is often performed at the printed circuit board (PCB) level prior to system testing. The PCB test might still be performed in a functional way, but by sub-dividing the problem, test preparation and diagnostics became more manageable. However, the rapidly increasing complexity of Integrated Circuits (IC) caused the same type of problems with PCB functional test as encountered at system-level; namely long test preparation times, uncertain fault-coverage, and poor diagnostics.

The next test method to be widely adopted was in-circuit testing (ICT). By providing direct electrical access to the components on a PCB via an electromechanical "bed-of-nails" fixture, it was possible to test for manufacturing faults. This technology was well suited for dual-in-line packages (DIP) and plated-through-hole PCB technology. But along with newer fine-line PCBs and more complex array-style IC-packages, such as QFP, BGA, CSP, FCA, etc., with higher pin-counts and smaller pitches, test access has become severely limited. Fixturing technology could not keep up with the ever-decreasing dimensions of pins and pitches and the higher pin-counts of packages.
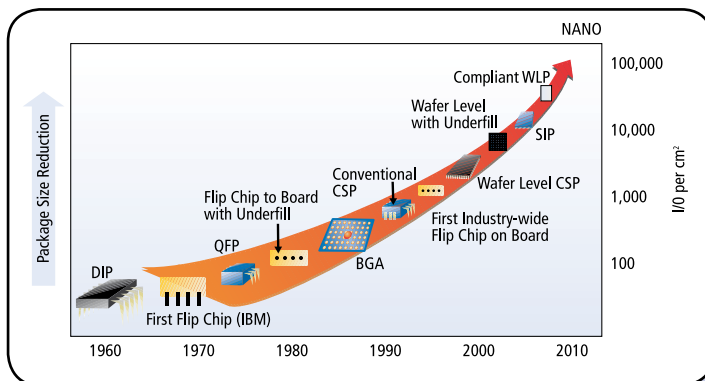

Figure 1. IC evolution leads to greater complexity and pin count

Fortunately, the industry anticipated these problems, and through a cooperative effort, the boundary-scan method was developed and adopted as the IEEE Standard 1149.1 Test Access Port (TAP) and Boundary-Scan Architecture. The objective of this powerful standard was to overcome many of the drawbacks of the other test technologies.

Figure 2. Increasing importance of DFT

Following this evolution in testing methods a number of observations can be made:

- Design-For-Testability (DFT) has become increasingly important with functional board testing in order to increase controllability and observability of the target's functionality during test. In order to be able to test today's state-of-the-art designs, DFT is mandatory.

- Initially, testing was a mixture of design debug and detection of manufacturing faults. As design complexity has increased, these tasks become more manageable if they are addressed separately. What is needed is a means of detecting and clearing prototype manufacturing faults prior to debugging the design.

- As product complexity has increased, many manufacturers have employed a multi-step test strategy whose aim is to detect and correct faults as early in the production process as possible.

Most test strategies follow the general sequence shown in Figure 3. After assembly and optical inspection and prior to functional testing, a structural test is usually performed to identify and correct any faults that may have been introduced during manufacturing, such as soldering opens and bridges and missing or incorrect parts. In general, a structural test can be prepared rapidly, in fact, often by automated software. Furthermore, as long as there are sufficient test points available, faults detected by a structural test are very quickly diagnosed for repair.
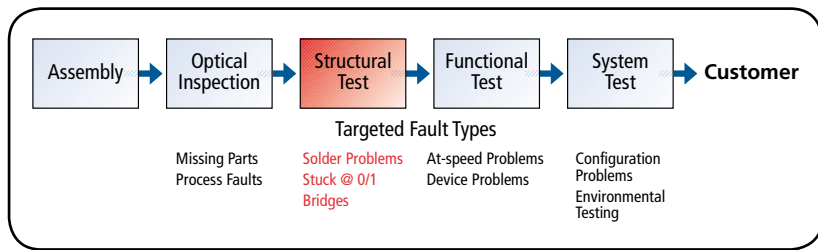

Assembly	Optical Inspection	Structural Test	Functional Test	System Test	Customer

Targeted Fault Types

Missing Parts	Solder Problems	At-speed Problems	Configuration Problems
Process Faults	Stuck @ 0/1	Device Problems	Environmental Testing
	Bridges		

Figure 3. Typical PCB test strategy

Because of the strengths of structural testing (speed of test development and precise diagnostics), it is desirable to find as many faults as possible at the structural test step, rather than allowing them to escape to functional. However, as stated above, this plan is effective only if the structural test is supported by enough test points to quickly identify the source of failures. With the increasing complexity of modern designs and assemblies, in order to achieve a high level of fault coverage, manufacturers are considering new structural test methods as well as the more traditional techniques.

Functional testing usually follows the structural test and is aimed at detecting operational problems such as those that might only occur at system speed or under particular user sequences, etc. One of the characteristics of functional testing is its vulnerability to changes in the design. Even a small design change can cause the entire test development effort to be wasted. Furthermore, because a functional test program is not focused on manufacturing types of faults, it may provide poor fault coverage. Also, the fault coverage of a functional test program is not known, unless cumbersome fault simulators are used.
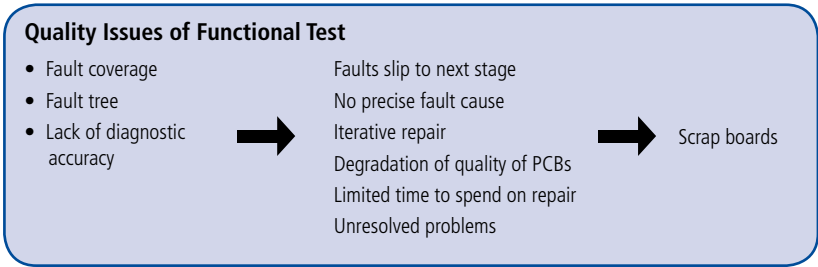
Due to a lack of automated tools, the functional test program and diagnostics are generally prepared by the designer who is the person with the most knowledge about this design. However, the designer's time is a scarce resource; it is often not feasible to generate a precise, down-to-the-pin level diagnostics routine, since that would take too much time. The result is an imprecise and lengthy diagnosis that will require trial and error repair methods. This will in turn detract from the quality / reliability of the delivered products.

Functional Test Characteristics

Test Preparation
- Vulnerable for design changes
- Difficult to focus on manufacturing faults
- Fault-coverage: Unknown unless complete fault simulation is performed

Diagnostics
- Diagnostics prepared by designer
- Design specific
- Fault tree

Quality Issues of Functional Test

- Fault coverage
- Fault tree
- Lack of diagnostic accuracy

➡

Faults slip to next stage
No precise fault cause
Iterative repair
Degradation of quality of PCBs
Limited time to spend on repair
Unresolved problems

➡

Scrap boards

Alternatively, if time limits are set to the repairs, the result could be a pile of scrap-boards with unresolved problems waiting to be debugged. In many cases, the problems are never solved, resulting ultimately in a waste of capital.

As previously mentioned, one of the most widely used structural test methods over the years is In-Circuit Testing (ICT), developed to complement the limitations of functional test. In ICT, electrical stimuli are driven onto the unit under test (UUT) and the results are captured by means of probes on a bed-of-nails test fixture. Standard sets of test vectors for each component result in a test program aimed at detecting manufacturing faults. Furthermore, ICT was capable of fault diagnostics at the component level by means of the bed-of-nails fixture.
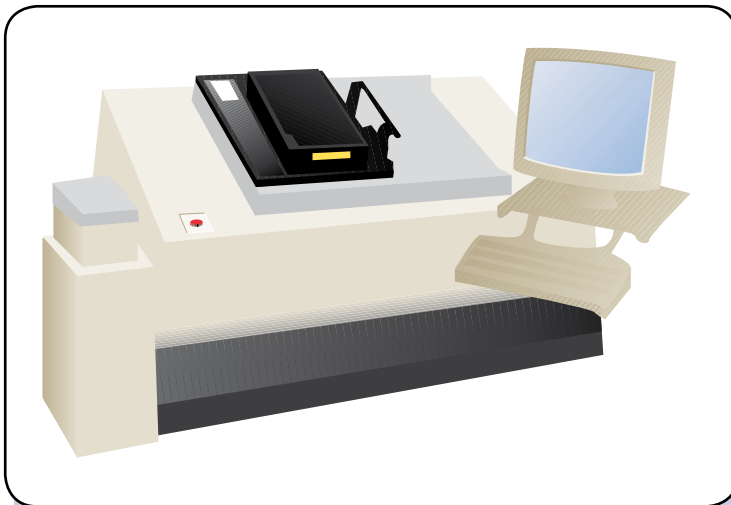

Figure 4. Typical In-Circuit Test system and bed-of-nails fixture

However, this type of fixture also has some drawbacks that can become prohibitive depending on the circuit technology in use.

• First, the bed of nails gives mechanical and logical access to internal circuit nodes. This intrusion in the logic, called back-driving, may have an adverse impact on the quality/reliability of the PCB, because of its inherent use of the devices outside their specifications.

• Another disadvantage of ICT fixtures is inconsistent contact performance. Particularly as circuit board geometries shrink, the fixture pins become more fragile and test results less reliable, contributing directly to increased production costs. The reliability degradation is especially pronounced when the factory has adopted a no-clean process in which flux buildup may occur in the fixtures.

- Design changes that result in re-routing PCB tracks often require repositioning of test points / vias causing rework or replacement of test fixtures developed for previous revisions. For this reason, bed-of-nails test fixtures are usually not developed until a PCB design has reached the pre-production phase, when the design should be stable and not subject to further layout iterations. Thus, ICT is usually not available to assist in prototype debugging, forcing the designer to resolve a mixture of structural, functional, and design problems.

- The advent of ASICs and VLSI has also diminished the advantages of the "standard test vector sets". When the libraries for these devices are not available or are late, ICT may have to be performed without them by simply using (empty) sockets.

- A further challenge for ICT within production came with the introduction of new IC packaging technologies such as Surface Mount Technology (SMT), Ball-Grid Arrays (BGA) and new assembly techniques such as Multi-Chip Modules (MCM), Flip-Chip-Attach (FCA), Chip-on-Board (COB) and Tape Automated Bonding (TAB). All these new technologies make the mechanical access as required for ICT difficult if not impossible.

In-Circuit Test Characteristics

Test Preparation

- Uses standard test sets for components
- Focused on manufacturing faults
- Bed-of-nails fixture per board type
- Fault-coverage: Satisfactory

Diagnostics

- Diagnostics on component level

Quality Issues of In-Circuit Test

- Overdrive technique may influence quality/reliability of product to be tested
- Testpads cause noise-sensitivity increase by extra capacitance
- Bed-of-nails fixture related problems
  - · Reproducibility of contacting
  - · No controlled wiring
- Increasing complexities for ASICs/VLSIs: Lack of (standard) test vectors
- Technology oriented resulting in degrading fault coverage (compromises!)

Test equipment vendors have continued to push ICT technology with the availability of testers capable of accessing in excess of 5,000 nodes. The corresponding bed-of-nails fixtures have become more expensive, heavy and subject to the reliability problems mentioned previously. Unfortunately, despite the advances in ICT, board manufacturers have experienced a steady decrease in test coverage, a result of the worsening imbalance between actual circuit nodes on the board and the number of accessible test fixture circuit nodes.

In recent years, several alternative structural test methods have been used by the manufacturing industry to provide complementary test coverage and to resolve the testing difficulties associated with complex SMT board designs.

In addition to boundary-scan, two alternative test techniques are automated x-ray inspection (AXI), which is capable of inspecting solder related process problems and automated optical inspection (AOI), aimed at detecting the presence, absence or misalignment of devices, as well as determining correct values of passive devices in some cases. However, neither AXI nor AOI has the ability to perform parametric measurements to verify that the correct passive components have been placed, a function best performed by in-circuit testing or flying probe testing.

The following diagram depicts the relative effectiveness of ICT, AXI, AOI, and boundary-scan in testing for the fault types that are most common in today's electronic assemblies:
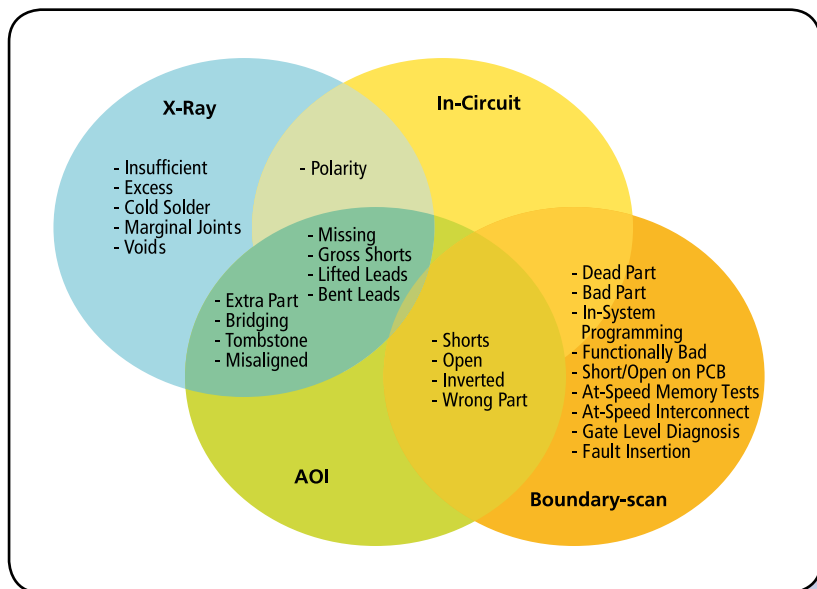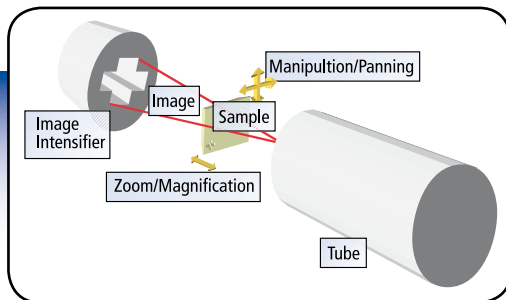

Figure 5. Fault types and test methodologies

Before examining boundary-scan as an advanced structural test method, we will first take a closer look at AXI and AOI.

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Over the last several years various forms of automated inspection have become popular, including x-ray techniques that allow invisible joints to be assessed. There is a wide range of equipment available, from manual systems that cost approximately $40,000 to fully automated systems costing over $500,000.

Figure 6. Principle of X-ray inspection

X-rays are generated from a microfocus x-ray tube and are transmitted through a beryllium window in the tube housing at the area where the component under investigation is located. Some of the x-rays are absorbed by the component and others pass through the component to a degree corresponding to the density of the material[1].

There are two principle types of x-ray systems, two-dimensional (2D) providing views in the X-Y plane as depicted in the diagram and 3D that also portray the Z dimension.

The gray scale images provided during x-ray inspection represent differences in the density of an object or in the thickness of the material being examined[2].

Figure 7. X-ray image of solder bridging fault

If 100% inspection of a solder joint is required, then the preferred option would be a fully automated system, which provides a far greater repeatability of results once the Pass/Fail criteria have been defined. Automated systems are also used in high volume/low mix facilities, in situations where the products are of high value, or if liability issues necessitate inspection.

A newer technique called x-ray laminography, originally developed by FourPye and now owned by Agilent Technologies, provides 3D capability by means of a cross-sectioning technique. The laminography system can inspect single- and double-sided surface mount assemblies including the area and height of solder joints providing a measure of the long-term viability of the interconnections.

Because x-ray inspection is relatively slow and requires a large initial investment, it is most often used by applying it only to a portion of the UUT, typically an area that may be prone to soldering problems. Also, analysis of AXI images can be subjective in nature and requires considerable training and experience.

Automated Optical Inspection (AOI)

Automated Visual Inspection (AOI) has been used for a number of years at the pre-reflow and post-reflow stages within the manufacturing process to verify the presence, absence, or misalignment of components. Ideally, pre-reflow AOI can contribute to statistical process control (SPC) techniques to achieve a "zero defect production line". It is important to remember that visual inspection can only observe the surface portions of the solder joints. Faults in solder joints beneath the dies, package substrates, PCB's etc., can only be detected through other techniques such as x-ray or boundary-scan.

AOI is based on a technique referred to as gray scale correlation[3] that stores an image considered to be an acceptable representation of the component to be inspected. The representative image is later compared to images obtained during production. However, problems may arise with gray scale correlation due to background color as depicted in the diagrams below, and inclusions in the image that may cause false errors[3].

Figure 8. AOI gray scale correlation

In order to improve the level of repeatability and robustness of AOI as required by the industry, a new solution called Vectoral Imaging has emerged that better supports inspecting PCB's on high beat-rate production lines. Vectoral Imaging is a pattern location search technology based on geometric feature extraction rather than absolute gray scale pixel values. By using geometric features, the image analysis is not affected by color changes or non-linear changes in size such as those found with components due to manufacturing variations.

To resolve the limited access problems associated with other structural test strategies, the IEEE 1149.1 Boundary-scan standard was developed as an alternative complementary test solution that provides

• High test coverage on complex PCB's

• Rapid test development cycles requiring minimal test fixturing

• Low-cost of ownership

• High diagnostic resolution

• High-performance in-system programming

Boundary-scan was first proposed in 1985 and became the IEEE 1149.1 standard in 1990. During the first few years after 1990, boundary-scan gradually gained in popularity as IC silicon vendors provided more devices compliant with the IEEE 1149.1 standard. At this time, a great many boundary-scan devices are available, and literally thousands of production lines around the world use boundary-scan routinely in board testing and in-system programming.

To comply with the standard, a device must include the 4-wire (5-wire if optional reset signal is included) Test Access Port (TAP), internal boundary-scan cells for each pin and associated internal boundary-scan registers and additional multiplexing circuitry. In addition, the device vendor must provide Boundary Scan Description Language (BSDL) files that fully describe the boundary-scan implementation in the associated devices.

Figure 9. Implementation of boundary-scan within the IC

What is needed for boundary-scan access?

The first requirement is to use boundary-scan compatible devices in your design. Because many ICs from a large number of silicon vendors have boundary-scan already built-in, this requirement is often easily met.

Moreover, to achieve good test coverage, it is not necessary to have all devices equipped with boundary-scan. For example, there may be clusters consisting of non-boundary-scan parts that will be testable despite the lack of direct boundary-scan access. In fact, practical examples exist in which an entire PCB is controlled, observed, and thoroughly tested (including memories) from just one or a small number of boundary-scan devices.

Figure 10. Boundary-scan incorporated on the printed circuit board

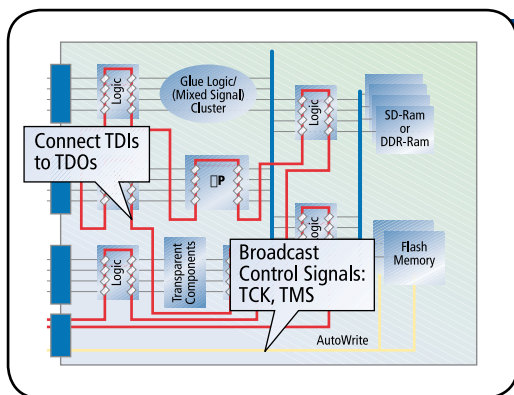Accessing the boundary-scan devices in your design is a simple matter. The boundary-scan components are interconnected in a chain (or multiple chains) on your board. This is done by sequentially connecting the boundary-scan data output pin (TDO) on one device to the boundary-scan data input pin (TDI) of the next device, and so on. To control this "test infrastructure" which includes the shifting operations etc., each boundary-scan device is connected to the test clock (TCK) and the test mode select (TMS) signal.

As for the other logic functions, normal design rules apply to the layout. To help you further, JTAG Technologies provides a booklet called "Board DFT Guidelines" describing in detail how to implement boundary-scan into your products. This booklet can be obtained free-of-charge via www.jtag.com.

What can be accomplished with Boundary-scan?

Boundary-scan was invented to overcome the manufacturing test access problems anticipated with in-circuit testing of SMT designs. In fact, several different types of tests can be conducted via boundary-scan as discussed in the following pages.

Moreover, manufacturing testing is not the only application for the serial bus and the Test Access Port (TAP). Due to the simple means of access for test purposes, the ease of test preparation and the low cost of the tools, boundary-scan is often successfully applied to testing prototypes for manufacturing faults. Without boundary-scan capability, prototype testing and debug may take several days or even weeks, consuming the scarce time of the designer. Furthermore, by using boundary-scan, the prototype test to screen out structural faults can be performed by production personnel, since no special knowledge is needed of the logic functions of the PCB.

In addition to board testing, the boundary-scan infrastructure can be used to program flash memory devices and PLDs after board assembly. Successful flash programming requires access to the address, data and control pins of the flash memory device via boundary-scan cells, a requirement which is usually easily met. The advantages of in-system programming are numerous:

- During prototyping, after clearing any manufacturing process faults, boundary-scan can be used by the design groups for firmware programming and verification of design functionality

- In production, elimination of pre-programming simplifies inventory management and reduces device handling

- Flexible customizing of the products is possible at the latest possible stage in the production

- Testing and device programming may be performed as one action using the same (test) equipment via the same connector

> **In-system Programming**
>
> Many different types of ICs can be programmed via boundary-scan:
>
> - Flash (NOR and NAND)
> - Serial Memories (SPI, I2C, SMBus, and Microwire)
> - PLDs and FPGAs

System level test access

System level testing is another example of an additional application area for boundary-scan. By extending the board level boundary-scan chain to the back plane, test access to the PCBs within a system level environment can be achieved. Hierarchical scan devices from National Semiconductor, Firecron, Texas Instruments, and Lattice Semiconductor can be used to select individual modules or sub-assemblies during the system test. System test execution can also be performed from an external tester or from internal system logic in the form of an embedded test controller.
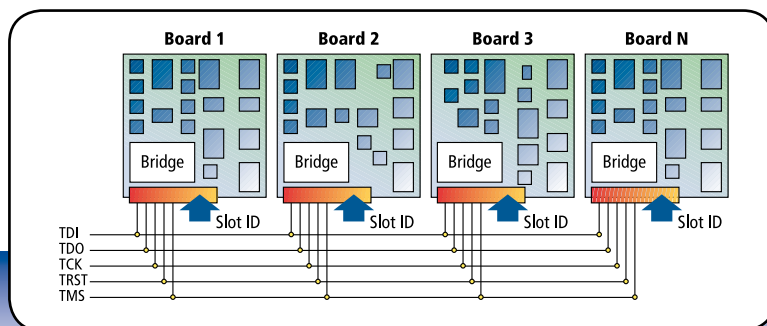

Figure 11. Use of bridging devices for multi-board boundary-scan access

Several solutions are available in the market to support these applications. The JTAG Technologies booklet, "System DFT Guidelines" describes the architectural considerations to implement boundary-scan at system level. This booklet can be obtained free-of-charge via www.jtag.com.

Embedded testing

Control of the boundary-scan test infrastructure can be embedded within the design of the system, enabling built-in self test (BIST) and remote testing and diagnostics, resulting in higher reliability and lower operational costs. Leading FPGA and specialist silicon vendors offer BIST capabilities with either re-configurable IP cores or hard-coded IP within commercial-off-the-shelf (COTS) products. These embedded test cores can be used by designers to provide an enhanced device level test capability not only to perform at-speed interconnect tests between devices and board interfaces, but to comprehensively test silicon and even detect and diagnose faults to gate level.

Environmental screening/Accelerated life testing

To increase the reliability of electronic systems, early life failures can be weeded out by burn-in or other stress techniques. PCBs may be operated at higher temperatures to accelerate the infant mortality period and cause early failures to occur. Common practice is for faults induced during the burn-in to then be diagnosed at room temperature using production test equipment such as in-circuit testers. In many cases, however, the fault may not occur at room temperature or may manifest itself differently than during burn-in.

Often, the reason for the discrepancy is the temperature sensitivity of weak solder joints. A connection which is open at high temperature may be restored as the board temperature is decreased, or as the bed-of-nails fixture applies force to it. Boundary-scan can significantly improve the effectiveness of the burn-in and reduce the possibility of failures in the field by allowing the testing and diagnostic process to take place at elevated temperature, due to the simple test interface.

Boundary-scan integration with ICT

A typical PCB manufacturing production line may consist of the process stages shown in the diagram below, a series of complementary inspection and test methodologies that ensures adequate defect coverage.

Many manufacturers, including contract manufacturers (CM's), are interested in integrating boundary-scan capability within one or more of their existing test steps. This desire may be driven by a need to obtain the benefits of boundary-scan in testing high-density PCBs without introducing an additional test stage within the existing flow line. Also, there may be a desire to include the operator functions for boundary-scan within familiar test systems.

Choosing between the many possible combinations of test and inspection methods (e.g. optical, x-ray, ICT and boundary-scan) depends on several factors including the characteristics of the product to be tested, production throughput requirements and the anticipated fault spectrum. Because boundary-scan is complementary to other test methods such as ICT, the combination provides an optimal test strategy with minimal cost and the maximum coverage for the anticipated fault types. However, the boundary-scan/ICT combination is not ideal for every application. For low-volume production it may be more cost effective to use a dedicated boundary-scan tester in conjunction with a flying probe tester to test passive analog components and other non-scan devices. Similarly, boundary-scan coupled with a manufacturing defect analyzer (MDA) may be sufficient for lower-cost or less complex consumer type products.

Another integration alternative is the combination of boundary-scan test capability within a functional test (FT) system. This method provides a unified platform for structural testing and in-system programming, followed by functional testing, under control of a single test executive.

A professional boundary-scan system will support all of the preceding combinations as well as stand-alone operation, allowing for straightforward porting of applications, developed and validated off-line, to the factory environment. To help users optimize their test strategies, JTAG Technologies provides users with a choice of production arrangements. Choices range from a stand-alone boundary-scan system to a wide variety of integration packages for third party test systems, including many in-circuit and flying probe testers as well as functional test systems using National Instruments LabVIEW, LabWindows, and TestStand.
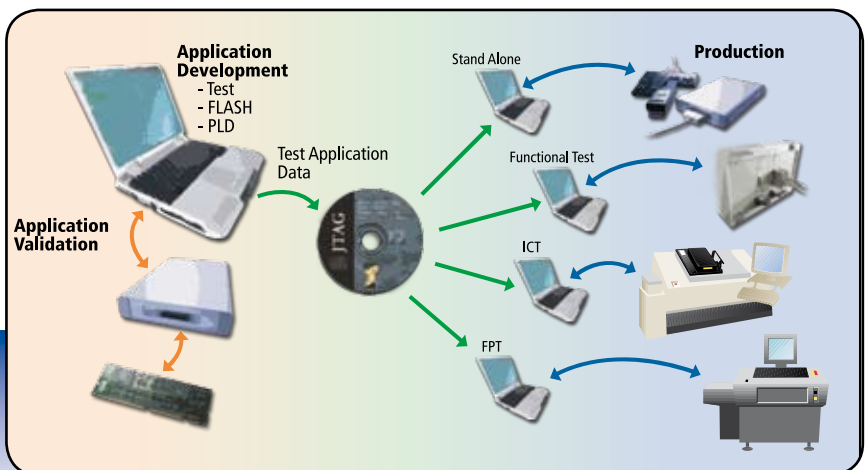

Figure 12. Variety of production implementation alternatives, stand-alone and integrated

Testing your tester

The board level boundary-scan infrastructure is an extension of the externally connected test controller. Since a fault in this section would interfere with testing the entire target board, the boundary-scan infrastructure should always be tested first and repaired before going on to subsequent boundary-scan tests. The diagram below indicates a typical sequence of boundary-scan operations, including testing and in-system programming. The sequences are easily customized to meet precise factory requirements.
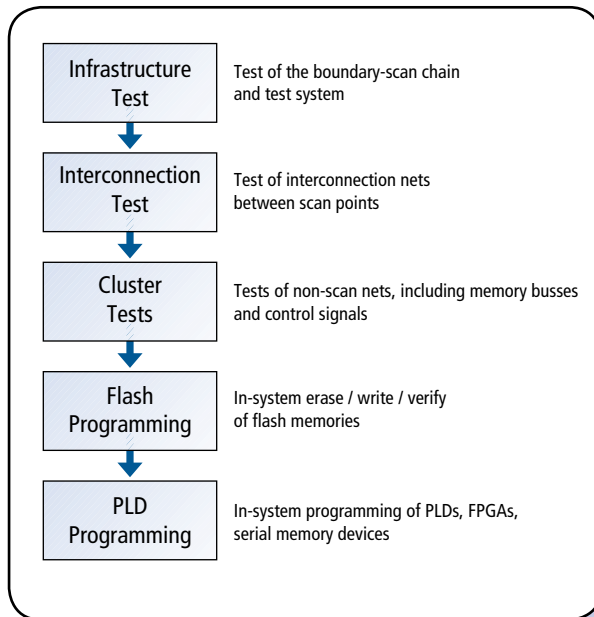
Infrastructure Test	Test of the boundary-scan chain and test system
Interconnection Test	Test of interconnection nets between scan points
Cluster Tests	Tests of non-scan nets, including memory busses and control signals
Flash Programming	In-system erase / write / verify of flash memories
PLD Programming	In-system programming of PLDs, FPGAs, serial memory devices

Figure 13. Typical boundary-scan application flow

Interconnection Testing

The next step in the boundary-scan test process is to verify the integrity of all boundary-scan testable interconnections (nets) on the PCB. A net is considered to be boundary-scan testable if it can be driven and sensed by boundary-scan cells of devices on the board, via the parallel connector pins of the board, or by boundary-scan compliant general-purpose I/O modules external to the board. The interconnection test covers a wide variety of net terminations; such as device drivers, sensors, tri-state outputs, bi-directional pins, pull-up/down resistors, differential nets and parallel I/O's.

The boundary-scan interconnect test verifies the electrical integrity between boundary-scan devices by shifting test patterns into the driver cells of the interconnection nets. Logical "1" and "0" values are transmitted from each driver through the associated bond wire, device pin, solder joint and board via to the interconnecting piece of track. At the other end of the net, the logic value is carried through the board via solder joint, device pin and bond wire to the receiving boundary-scan cell as depicted on the diagram below.

Thus, it can be seen that the boundary-scan interconnection test is much more comprehensive than an ICT bed-of-nails test between a pair of physical test probes contacting the bottom surface of the board.
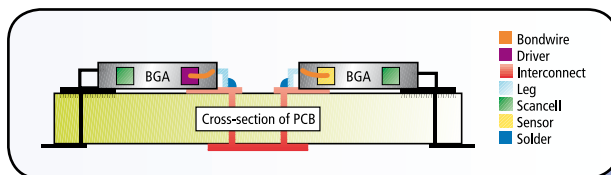

Figure 14. Detecting connection faults between ICs

Achieving Test Access to Clusters

Most PCBs consist of a mixture of devices that comply with boundary-scan and others that do not comply. In order to achieve high test coverage on such boards, it is very desirable to extend boundary-scan testing beyond just the interconnections between compliant ICs. The diagram below illustrates a PCB with different types of non-boundary-scannable devices, referred to as clusters. Using scan access to the primary input/output pins of the clusters, testing for typical manufacturing faults such as bad solder joints, solder bridges or defective components on PCBs or defective wire bondings on multi-chip modules inside a cluster, can be readily accomplished.

Typical clusters that can be tested during prototype debugging and manufacturing are glue logic and memories. Often, the presence of just a small number of boundary-scan components (e.g. a microprocessor) on the board provides sufficient access to achieve a high degree of test coverage.

Memory Cluster Testing

A specific case of cluster testing is the validation of connectivity to memory devices on the PCB such as static and dynamic memory devices including SRAM, DRAM, SDRAM, and FIFOs. In many cases, boundary-scan techniques are capable of testing for all possible manufacturing defects that could impact the memory address and data busses and control signals. In addition, a fault dictionary is generated containing all the necessary information for full diagnostics.

Economic Benefits

The advantages of boundary-scan that have been discussed earlier can be translated into solid commercial benefits by shortening critical manufacturing processes and hence the time-to-market, by savings in capital investment, and by reducing the cost of ownership.

a) Shorter Time-to-Market

The significant benefit of reducing time-to-market on profitability has been documented in various studies. One such study reveals that, on average, after-tax profit is adversely impacted by 33% when a product is shipped six months late, as compared to

> **Economic Benefits**
> - Shorter time-to-market
>   · Concurrent engineering
>   · Reduced time for proto-type debugging
>   · Faster production ramp-up
> - Lower costs
> - Improved product quality and reliability

only a 3.5% reduction of profit, when the product development expenses are overspent by 50%.[6] Also, the faster a product is introduced into a competitive market, the longer will be the potential lifetime and hence the greater its return on investment.
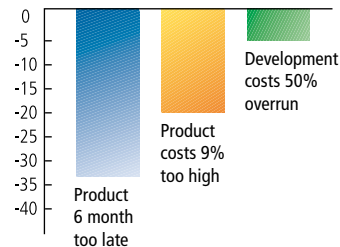
Boundary-scan improves the time-to-market of a product in the following ways:

- Prototype debug is quicker, due to the use of boundary-scan to detect structural faults
- Test development is shortened by the availability of advanced pattern generation tools
- PCB testability is quantifiable during the design phase, allowing optimization to take place before any layout activity is undertaken and possibly reducing the number of design cycles
- In-system programming of flash and PLDs allows quicker programming and re-programming during the development and production processes.
- ICT fixtures are eliminated or reduced in complexity, shortening the production engineering time i.e. faster production start-up
- Fewer defective boards escape to functional test, saving valuable engineering and reducing the time needed for diagnostics and repair

% Loss in Profit After tax

- Product 6 month too late
- Product costs 9% too high
- Development costs 50% overrun

Assumptions:
- 20% growth rate in market
- 12% annual price erosion
- 5 year product life cycle

Concurrent Engineering

Corporate management commits to introduce concurrent engineering in order to get the right product to market at the right time, for the right price. Ideally, the project team consisting of representatives from design, production, test engineering, and marketing meets regularly, seeking to avoid redesigns due to problems that could affect manufacturing or other functional areas.

As a result, significant life cycle cost savings are realized, more than justifying the extra time spent in the design phase. If a redesign becomes unavoidable, then it is done in such a manner as to fit the design into the current manufacturing process, rather than the opposite, avoiding unnecessary costs.

Boundary-scan is well-suited to a concurrent engineering approach to product development. Test engineering effort during the design phase ensures that the product can be tested thoroughly throughout the product life cycle.

Employing boundary-scan DFT principles eliminates the need to develop complex functional test routines to test the product, providing much improved test coverage and diagnostic resolution, and helping to avoid lengthy debug and rework cycles.

Experience has shown that concurrent engineering significantly shortens product development time, while boundary-scan testing improves test coverage and test development cycle time, minimizing the time to market.

Reduced Time for Prototype Debugging

The design faults encountered in prototype debug are often mixed in with manufacturing-related faults such as shorts and opens. However, at this point in the development, investment in specialized or dedicated test equipment such as fixtures is usually held to a minimum due to the interim nature of the prototype stage. As a result, prototype debugging is usually performed with ad-hoc functional test systems in which fault detection and diagnostic resolution are difficult and time-consuming.

Boundary-scan testing can dramatically improve this situation. As shown in the following diagram, the test programs for manufacturing faults can be easily developed in time to help the designer debug the prototype PCB design. This is especially beneficial in the design of large systems where considerable numbers of prototypes are required for further development of the system software or the product hardware/software integration. The reduction of this critical path contributes significantly in meeting the time-to-market objectives. Furthermore, the same boundary-scan test used for prototype debug can be re-used at several other points in the product life cycle.
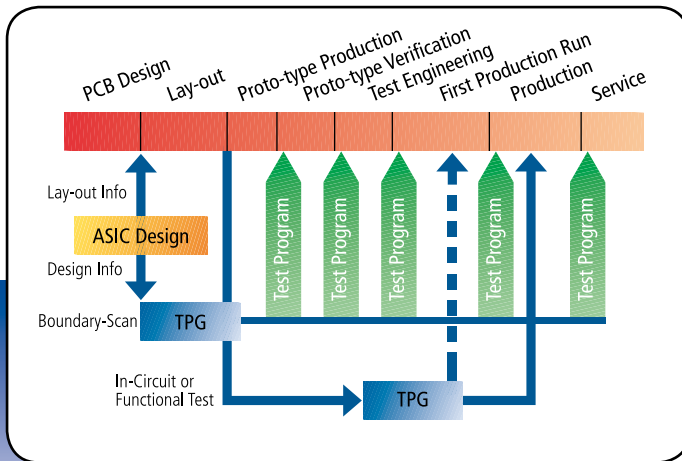
Figure 15. Boundary-scan can be used earlier and in more steps of the life cycle than conventional test methods

Quicker Production Ramp-up

Production start-up problems in the factory can jeopardize the scheduled introduction of a new product. The assistance of the designer may be requested, which is inefficient in at least two ways:

- The dedicated test equipment of the designer is not well-suited to supporting the production line
- Re-assigning designers to production support impacts their primary function of product development, thereby delaying other projects

Moreover, such a working method does not guarantee high quality and leads to overspent budgets.

The previous section demonstrates the value of applying boundary-scan and having test patterns available before prototyping starts, helping ensure that prototype production and test preparation are completed on time.

Lower Costs
- Lower capital investments
  - · Price of BST tester much lower
  - · For BST less testers needed
- Test preparation less and once
- Shorter fault diagnosis times
- Fault coverage higher

b) Lower capital investment

As discussed previously, the introduction of Boundary-scan Test technology also implies the application of DFT and concurrent engineering. These disciplines have only a moderate impact on the investment requirements for automated design support. In many cases, existing CAD/CAE facilities and software can easily be supplemented with the tools needed for boundary-scan test pattern generation and fault coverage analysis. This level of capital investment has an immediate positive impact on productivity by supporting rapid test development based on schematics input, avoiding tedious manual data entry and assuring the quality of data transfer.

The introduction of boundary-scan testing further reduces the investments for testing, particularly in the manufacturing phase of the product life cycle. This reduction has three causes:

- A boundary-scan test system is much less expensive than a traditional ICT tester, roughly an order of magnitude lower.
- Costly fixtures are either eliminated or simplified, resulting in savings that multiply with each board type to be tested.
- Fewer testers may be needed due to shorter fault diagnosis times, which in turn allow the factory throughput per tester to be increased

c) Lower cost of ownership and improved product quality and reliability

Scan as a corporate design rule.
Establishing boundary-scan as a corporate design rule to support DFT implies that the designers will consider production issues before the design begins. Innovative solutions are fostered before legacy implementations can block them. These phenomena contribute to the improvement of quality, reliability, and testability of the electronic products and systems.

Improved Product Quality and Reliability
- Mandatory design rule
- Technology compliance
- In time availability of manufacturing test
- Quality of test and diagnostics

Technology compliance. An inherent characteristic of boundary-scan testing is the compatibility between the product to be tested and the test equipment. This results from boundary-scan being embedded in the logic of the functional design. There is never a mismatch or divergence of technologies as can happen with bed-of-nails systems, in which a conflict may arise between fixture engineering and the shrinking device sizes and novel packaging technologies. These conflicts can clearly influence the quality of testing and consequently the product quality.

In-time availability of manufacturing tests. Because of the short test preparation lead times, boundary-scan tests are ready prior to manufacturing start-up. The benefits are the avoidance of ad-hoc test methods and immediate use of the standard test procedures. In contrast, traditional functional or in-circuit test programs are often either not available in time or do not offer high fault coverage at the outset of manufacturing. The impact of these shortcomings on a customer's expectations and your brand name and service costs can be disastrous for the long-term growth of your company!

Boundary-Scan Benefits in Practice

By Industry Reported Example

- Test generation time decreased from 1 month to 5 days
- Test debug times decreased from 1.5 weeks to 5 hours
- Pin-level fault coverage increased from 40% to 95%
- Fault isolation times decreased from 1 hour to 5 minutes
- Test maintenance and support times decreased from 30 minutes to 5 minutes per month
- Prototype designs tested at 90% pin level fault coverage
- Prototype returned to respective designer within 48 hours after receipt of an assembled module

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Quality of test and diagnostics. The very high fault coverage of the boundary-scan test and the high degree of diagnostic capabilities lowers the rate of faults that are undiscovered during the manufacturing phase, resulting in an improved product quality and reliability.

How can you determine if boundary-scan makes sense for your operation? If the issues and problems described previously sound familiar to you, then consider the following checkpoints as they apply to your situation:

a) Do you have one or more devices in the design available with boundary-scan? For example:

- Your own ASIC(s) designed with boundary-scan
- Complex CPLDs
- Complex processor chips
- Digital signal processors
- Telecomm/datacomm devices

b) Do you want to perform in-circuit or in-system programming of CPLD's or flash memory devices in your factory in order to simplify process flow and logistics?

c) Do you have problems with physical access (fixtures) with ICT, due to fine pitch surface-mounted devices such as ball-grid array or other complex package types?

d) Are you using only functional testing, because the ICT methodology is too expensive for the (low) number of boards in your activity?

e) Are your test development costs and manufacturing time for fixtures and in-circuit test programs becoming unacceptably high?

f) Do your hardware designers want to spend less time debugging prototype boards due to production faults?

g) Do your engineers have insufficient time to spend designing functional tests with adequate coverage for detecting production faults?

h) Do you want to re-use the efforts in time and investments spent testing during the prototype-debugging phase for manufacturing testing and for through-life testing?

i) Is your activity:

- A small or medium size electronics company
- A department or activity within a large company such as prototype production, test engineering, or quality assurance
- An engineering/instrumentation department of an Institute/University
- An engineering department of contract manufacturing company

j) Is minimizing the time-to-market of your products vital for your company?

k) Is meeting project deadlines/milestones and reducing unexpected process problems very important for your organization?

l) Do you have too many scrap boards in your production that cannot be repaired due to lack of diagnostics?

m) Does the required quality of your products preclude repeated repair actions?

If one or more of the previous points are valid for your situation, you may want to consider boundary-scan as an applicable solution, and we encourage you to contact us for more specific information. We would be pleased to arrange a demonstration of the power of boundary-scan as well as to arrange a review of your design and the applicability of this technology. Our experts are ready to help you.

Please visit our website www.jtag.com for information about JTAG Technologies and our complete product line of development and production tools for:

- Prototype debugging
- Manufacturing testing
- System testing
- Repair
- In-system programming of flash memories or CPLD devices

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ASIC	Application Specific IC
AOI	Automated Optical Inspection
AXI	Automated X-Ray Inspection
BGA	Ball Grid Array
BSDL	Boundary-Scan Description Language
BST	Boundary-Scan Test
UUT	Unit under test
CAD	Computer Aided Design
CAE	Computer Aided Engineering
CEM	Contract Electronic Manufacturer
COB	Chip On Board
CPLD	Complex Programmable Logic Device
DFT	Design For Testability
DIL	Dual In Line
DLL	Dynamic Link Library
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DUT	Device Under Test
EDIF	Electronic Design Interchange Format
FBT	Functional Board Test
FCA	Flip Chip Attach
FIFO	First In First Out
FPT	Flying Probe Tester
IC	Integrated Circuit
ICT	In Circuit Test(ing)
IEEE	Institute of Electrical and Electronics Engineers
ISDN	Integrated Services Digital Network
JTAG	Joint Test Action Group
MCM	Multi Chip Module
MTBF	Mean Time Between Failures
PCB	Printed Circuit Board
PLD	Programmable Logic Devices
PTH	Plated Trough Hole
QFP	Quad Flat Pack
RAM	Random Access memory
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Synchronous Random Access Memory

SMT	Surface Mount Technology
TAB	Tape Automated Bonding
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TPG	Test Pattern (or Program) Generation
TRST	Asynchronous Test Reset
VLSI	Very Large Scale Integration

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